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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/518,709	03/03/2000	Takahisa Yamaha	P/2171-180	5749

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EXAMINER
ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/518,709	Yamaha
Examiner	**Art Unit**
Edgardo Ortiz	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 8, 2002*.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *14-28* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *14-28* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to an amendment filed April 13, 2002 on which Applicant canceled claims 1-13 and added new claims 22-28.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14-19 and 21 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takahisa et.al. (Japanese Patent No. 08-222633) in view of Jeng (Japanese Patent No. 10-074755). With regard to Claim 14, Takahisa teaches a semiconductor substrate (10), a MOS type transistor formed on said semiconductor substrate, including a source (S), a gate (G) and a drain (D), an interlayer insulating film (14) formed on the semiconductor substrate, covering the MOS transistor, a wiring layer (19) formed on said interlayer insulating film and a hydrogen transmission preventing film (28) covering said MOS type transistor and said wiring layer.

However, Takahisa fails to teach that the interlayer insulating film includes a hydrogen resident film. Jeng teaches a semiconductor device including an interlayer insulating film (18) including a hydrogen resident film. Therefore, it would have been an obvious modification to someone with

ordinary skill in the art, at the time of the invention, to modify the structure as taught by Takahisa to include an interlayer insulating film having a hydrogen resident film, in order to increase crack suppression of the device layers and the resistance force to high temperature processes.

With regard to Claim 15, a further difference between Takahisa and the claimed invention is a hydrogen resident film containing hydrogen silsesquioxane resin. Jeng teaches a semiconductor device including an interlayer insulating film (18) including a hydrogen resident film and containing hydrogen silsesquioxane resin (HSQ). Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Takahisa to include a hydrogen resident film containing hydrogen silsesquioxane resin, in order to provide a low-k insulator and to increase crack suppression of the device layers and the resistance force to high temperature processes.

With regard to Claim 16, Takahisa teaches a hydrogen transmission preventing film (28) including a silicon nitride film.

With regard to Claim 17, Takahisa teaches a wiring layer (19) having a lamination structure of Ti/Al alloy/TiN.

With regard to Claim 18, Takahisa teaches a wiring layer (19) having a lamination structure of Ti/Al-Si-Cu/TiN.

With regard to Claim 19, Takahisa teaches a wiring layer (19) including a plurality of wiring layers (16, 17) and a hydrogen transmission preventing layer (28) formed as thick as can to form a groove between adjacent wiring layers.

With regard to Claim 21, Takahisa teaches a hydrogen supply path for supplying the channel region of the MOS type transistor formed between the channel region and the insulating film (14).

Claims 20 and 22-28 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Takahisa et.al. (Japanese Patent No. 08-222633) in view of Jeng (Japanese Patent No. 10-074755) and further in view of Bai et.al. (U.S. Patent No. 5,861,340). With regard to Claims 20 and 22, Takahisa teaches a semiconductor substrate (10), a MOS type transistor formed on said semiconductor substrate, including a source (S), a gate (G) and a drain (D), an interlayer insulating film (14) formed on the semiconductor substrate, covering the MOS transistor, a wiring layer (19) formed on said interlayer insulating film and a hydrogen transmission preventing film (28) covering said MOS type transistor and said wiring layer.

However, Takahisa fails to teach that the interlayer insulating film includes a hydrogen resident film. Jeng teaches a semiconductor device including an interlayer insulating film (18) including a hydrogen resident film. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Takahisa to include an interlayer insulating film having a hydrogen resident film, in order to increase crack suppression of the device layers and the resistance force to high temperature processes.

A further difference between the claimed invention and Takahisa and Jeng is, silicide layers formed on the silicon gate electrode and the source/drain regions. Bai teaches a semiconductor device including a MOS transistor having a silicon gate electrode (204), source/drain regions (216) and silicide layers (220) on the silicon gate electrode and the source/drain regions. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as suggested by the teachings of Takahisa and Jeng to include silicide layers formed on the silicon gate electrode and the source/drain regions, as clearly suggested by Bai, in order to decrease the resistance of the gate electrode.

With regard to Claim 23, a further difference between Takahisa and the claimed invention is a hydrogen resident film containing hydrogen silsesquioxane resin. Jeng teaches a semiconductor device including an interlayer insulating film (18) including a hydrogen resident film and containing hydrogen silsesquioxane resin (HSQ). Therefore, it would have been an obvious

modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Takahisa to include a hydrogen resident film containing hydrogen silsesquioxane resin, in order to provide a low-k insulator and to increase crack suppression of the device layers and the resistance force to high temperature processes.

With regard to Claim 24, Takahisa teaches a hydrogen transmission preventing film (28) including a silicon nitride film.

With regard to Claim 25, Takahisa teaches a wiring layer (19) having a lamination structure of Ti/Al alloy/TiN.

With regard to Claim 26, Takahisa teaches a wiring layer (19) having a lamination structure of Ti/Al-Si-Cu/TiN.

With regard to Claim 27, Takahisa teaches a wiring layer (19) including a plurality of wiring layers (16, 17) and a hydrogen transmission preventing layer (28) formed as thick as can to form a groove between adjacent wiring layers.

With regard to Claim 28, Takahisa teaches an interlayer insulating film (14) that constitutes a hydrogen supply path between the hydrogen containing film, such as the one taught by Jeng, and the silicon substrate (10) under the gate insulating film (ox).

Response to Arguments

2. Applicant's arguments filed on April 8, 2002 have been fully considered and are addressed below. Applicant argues, regarding the rejection of claims 14-21, that the teachings of Takahisa and Jeng fail to teach the claimed invention. The examiner disagrees, and notes that as stated supra, Takahisa teaches a semiconductor substrate (10), a MOS type transistor formed on said semiconductor substrate, including a source (S), a gate (G) and a drain (D), an interlayer insulating film (14) formed on the semiconductor substrate, covering the MOS transistor, a wiring layer (19) formed on said interlayer insulating film and a hydrogen transmission preventing film (28) covering said MOS type transistor and said wiring layer. Jeng teaches a semiconductor device including an interlayer insulating film (18) including a hydrogen resident film. Therefore, the claimed structure is clearly suggested by the teachings of Takahisa and Jeng. Applicant further argues that Jeng teaches a HSQ film that releases hydrogen, but the hydrogen once released, is blocked by wiring and a capping layer and thus does not provide a hydrogen to the channel region. Nonetheless, the Jeng reference was cited to show a structure having an interlayer insulating film including a hydrogen resident film, which in combination with the structure of Takahisa having an interlayer insulating film and a channel region path, clearly discloses the

claimed structure. Lastly, Applicant argues neither of the cited references teach the formation of a silicide layer on a gate electrode and on source/drain regions. The newly cited Bai reference, as stated supra, clearly teaches a semiconductor device including a MOS transistor having a silicon gate electrode (204), source/drain regions (216) and silicide layers (220) on the silicon gate electrode and the source/drain regions.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7724. In case the Examiner can not be reached through a direct telephone call, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application should be directed to the Group 2800 receptionist whose telephone number is (703) 308-0956.

EO / AU 2815

6/12/02

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